JAPANESE PATENT OFFICE
PATENT JOURNAL
KOKAI PATENT APPLICATION NO. HEI 6[1994]-5778

Technical Disclosure Section

Int. Cl.[5]:	H 01 L 25/065 25/07 25/18 H 01 L 25/08 23/52 H 01 L 23/52 27/00
Sequence Nos. for Office Use:	8418-4M
Application No.:	Hei 4[1992]-161386
Application Date:	June 19, 1992
Publication Date:	January 14, 1994
No. of Claims:	9 (Total of 5 pages)
Examination Request:	Not requested

SEMICONDUCTOR DEVICE

Inventor: Masanobu Mizukoshi
Fujitsu, Ltd.
1015 Kamiodanaka,
Nakahara-ku,
Kawasaki-shi,
Kanagawa-ken

Applicant: 000005223
Fujitsu, Ltd.
1015 Kamiodanaka,
Nakahara-ku,
Kawasaki-shi,
Kanagawa-ken

Agent: Tadahiko Ito,
patent attorney,
and 2 others

[There are no amendments to this patent.]

Abstract

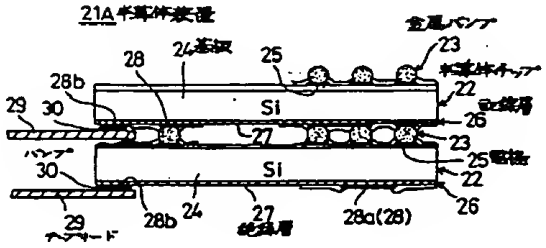
Objective

The present invention relates to a semiconductor device in which a plurality of semiconductor chips is arranged three-dimensionally, and the objective is to make positioning of each semiconductor chip easy by improving the junction strength, heat radiation property, and insulation property.

Constitution

Electrode (25) is formed on the element area surface of substrate (24) composing semiconductor chip (22), and metal bump (23) is provided on said electrode (25). On the other hand, wiring layer (26) formed with electrode pads (28a) and (28b) and optionally patterned wiring part is formed on the back surface. Then, metal bump (23) formed to electrode (25) of another semiconductor chip (22) front surface is joined to electrode

(28a) of wiring layer (26) formed on the back surface of one semiconductor chip (22), and is composed by being laminated successively.



Constitutional diagram of the first application example of this invention.

Key: 21A Semiconductor device
22 Semiconductor chip
23 Metal bump
24 Substance
25 Electrode
26 Wiring layer
27 Insulating layer
29 Chip lend
30 Bump

Claims

1. A semiconductor device characterized by the fact that in a semiconductor device in which a plurality of semiconductor

chips (22) formed with a prescribed number of electrodes (25) on the surface are patterned by being arranged three-dimensionally,

wiring layer (26) provided with a wiring part of prescribed pattern and a prescribed number of electrode pads (28a) and (28b) for external connection and internal connection is formed by interposing an insulation layer to the back surface of said semiconductor chip (22),

external connecting means (29) is provided to said electrode pad (28b) for external connection along with providing connecting means (23) to said electrode (25) on said semiconductor chip (22) front surface, and

said connecting means (23) in another semiconductor chip (22) is connected to electrode pad (28a) for internal connection on one semiconductor chip (22) back surface and a prescribed number are superimposed.

2. A semiconductor device noted in Claim 1, characterized by the fact that out of said semiconductor chips (22) laminated by a prescribed number, wiring layer (26) is not formed on the back surface of semiconductor chip (22) at the lowest part and a substrate formed with said wiring layer (26) is positioned at the top part of said semiconductor chip (22) at the highest part.

3. A semiconductor device noted in Claim 1 or 2, characterized by the fact that said connecting means is composed as metal bump (23).

4. A semiconductor device noted in Claims 1-3 characterized by the fact that said metal bump (23) is provided by being electrically contacted to said electrode (28a) on the back surface of said semiconductor chip (22) and being fixed according to the setting and contraction of the resin filled between semiconductor chips (22).

5. A semiconductor device noted in Claims 1-4 characterized by the fact that said external means is tape lead (29).

6. A semiconductor device noted in Claims 1-5 characterized by the fact that said packaging is executed with mold resin and said mold resin is interposed between a prescribed number of said semiconductor chips (22).

7. A semiconductor device noted in Claims 1-6, characterized by the fact that said electrode (25) on said semiconductor chip (22) front surface includes an electrode which does not participate in the circuit constitution of said semiconductor chip (22).

8. A semiconductor device noted in Claims 1-7, characterized by the fact that a prescribed number of heat radiating members (31a) and (31b) are positioned on said semiconductor chips (22).

9. A semiconductor device noted in Claim 8, characterized by the fact that said heat radiating member (31a) is formed with a prescribed number of conducting means (33)-(35) for connecting said semiconductor chips (22).

* * *